BIDIRECTIONAL WIRE I/O MODEL AND METHOD FOR DEVICE SIMULATION

ABSTRACT OF THE DISCLOSURE

A system and method is provided to accurately model bidirectional wire I/O using hardware description language (HDL). The preferred model and method uses an HDL model that provides two parallel paths between ports of the bidirectional wire I/O. During simulation, the ports are monitored for activity. When an event is detected on either port, the model checks both ports to see if they are different values. If the ports are different values, one of the two parallel paths is enabled and the other disabled. For example, the model enables the path in which the new signal has appeared and thus passes the signal to the other port. The preferred model allows for the use of HDL elements that support full timing annotation. The preferred embodiment also removes the possibility of high impedance transition error that can result from false transitions to a high impedance state.